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Applicant: Fujitsu Ltd.

SPECIFICATION

1. Title of the Invention

Complementary MOS Integrated Circuit

2. Scope of the Claims for Patent

1) A complementary MOS integrated circuit characterized in that a complementary construction is formed by an MOS transistor of one conductivity type channel, which is formed in a first one conductivity type channel forming region in an accumulation mode, and an MOS transistor of an opposite conductivity type channel, which is formed in a second one conductivity channel forming region in an inversion mode.

2) A complementary MOS integrated circuit according to claim 1, characterized in that a carrier density of said first one conductivity type channel forming region is higher than that of said second one conductivity type channel forming region.

3) A complementary MOS integrated circuit according to

claim 1 or 2, characterized in that a potential which is different from that applied to said second one conductivity type channel region is applied to said first one conductivity type channel region through a capacitor.

3. Detailed Description of the Invention

[Summary]

In a complementary MOS integrated circuit, by using an MOS transistor of one conductivity type channel formed in a one conductivity type channel forming region in an accumulation mode, the channel forming regions of two transistors constructing a complementary type are set to the same conductivity type.

[Industrial Field of Application]

The present invention relates to a complementary MOS integrated circuit.

The complementary MOS integrated circuit (COMS) has been used as a circuit forming an inverter in a logic integrated circuit in many cases.

The CMOS is constructed by combining two MOS transistors of an n-channel and a p-channel. Since the conventional construction has such difficulty that the manufacturing process is complicated or the like, it is desired to relieve the difficulty.

[Prior Art]

Fig. 3 is a schematic sectional side elevation view of an example of a conventional CMOS.

In the diagram, reference numeral 11 denotes a p-type silicon substrate; 12 an n-type well; 13 a field insulating film; 14a and 15a a source and a drain of a p^+-type; 14b and 15b a source and a drain of an n^+-type; 17a and 17b gates; 18 a gate insulating film; Vdd a power voltage; and Vss a substrate voltage.

The source 14a, drain 15a, and gate 17a construct a transistor T1a (enhancement type p-channel MOS transistor) in the well 12 as a channel forming region. The source 14b, drain 15b, and gate 17b construct a transistor T1b (enhancement type n-channel MOS transistor) in the substrate 11 as a channel forming region.

As for the CMOS, therefore, the circuit diagram is as shown in Fig. 4 and the operation is as shown in Table 1. The CMOS constructs an inverter of a low electric power consumption.

As another conventional CMOS, there is a CMOS in which each semiconductor region is set to the opposite conductive type and the polarities of the power voltage Vdd and substrate voltage Vss are set to the opposite polarities. It is similar to the above CMOS except for a structure in which the p-channel and n-channel are replaced with each

other.

Table 1 Operation of conventional CMOS

Input	State of T1a	State of T1b	Output
H	OFF	ON	L
L	ON	OFF	H

Where, H: high level

L: low level

[Problems that the Invention is to Solve]

In the CMOS with the above construction, however, since the conductivity type of each of the source 14a and drain 15a of the transistor T1a is opposite to that of each of the source 14b and drain 15b of the transistor T1b, the gates 17a and 17b, sources 14a and 14b, and drains 15a and 15b are formed as different structures on the transistor T1a side and the transistor T1b side. Accordingly, there is a drawback that the manufacture is complicated.

Owing to the presence of an N-P-N-P junction including a P-N junction of the substrate 11 and the well 12, latch-up caused by a thyristor operation is easily generated. Therefore, there is a problem that a latch-up countermeasure (not shown) is needed.

[Means for Solving the Problems]

The above problems are solved by a CMOS according to the invention, in which a complementary construction is formed by an MOS transistor of one conductivity type channel formed in a first one conductivity type channel forming region in an accumulation mode and an MOS transistor of an opposite conductivity type channel formed in a second one conductivity type channel forming region in an inversion mode.

[Operation]

In the conventional CMOS, since each of the two transistors T1a and T1b is the MOS transistor of the enhancement type, namely, in which the channel is formed in the inversion mode, the channel forming regions are set to an n-type and a p-type, respectively. The respective source and drain are set to a p-type or an n-type that is opposite to the conductivity type of the channel forming region. Accordingly, it is related to the above difficulty and problem.

In case of forming a CMOS in which one transistor is set to an MOS transistor in which a channel is formed in an accumulation mode, namely, of an accumulation type, in each of the transistors, the channel forming region is set to one conductivity type and the source and drain are set to

the opposite conductivity type.

It follows that it is unnecessary to form the gates, sources, and drains as different structures on the respective transistor sides and an N-P-N-P junction which causes latch-up is also allowed to disappear.

In this instance, in the above accumulation type MOS transistor, although an input voltage to the gate which is turned on is different from a conventional corresponding input voltage, by increasing a carrier density in the channel forming region and, if necessarily, by applying a potential different from that of the channel forming region of the enhancement type MOS transistor through a capacitor as will be described hereinlater, such a change in input voltage can be reduced.

As mentioned above, though the present CMOS operates as an inverter in a manner similar to the conventional CMOS, the manufacture is simplified and no latch-up may be generated.

[Embodiment]

An embodiment of a CMOS according to the invention will now be described with reference to a schematic sectional side elevation view of Fig. 1 and a circuit diagram of Fig. 2.

The embodiment shown in Fig. 1 utilizes an SOI

(Silicon On Insulator) structure.

In Fig. 1, reference numeral 21 denotes a p-type silicon substrate; 22 an n-type well formed in the substrate 21; 23 a silicon dioxide (SiO_2) insulating film on the substrate 21; 24a and 24b n^+-type sources; 25 an n^+-type drain; 26a and 26b p-type channel forming regions; 27a and 27b gates; 28 a gate insulating film; Vdd a power voltage; and Vss a substrate voltage.

The sources 24a and 24b, drain 25, and channel forming regions 26a and 26b are formed as one island made of silicon. A carrier density in the channel forming region 26a is higher than that in the channel forming region 26b. Respective dose amounts of boron (B) upon ion implantation in the regions are equal to about $2\times10^{13}/cm^3$ and $2\times10^{11}/cm^3$ (in both the regions, the accelerating energy is equal to about 35 KeV).

The source 24a, drain 25, channel forming region 26a, and gate 27a construct a p-channel MOS transistor T2a of an accumulation type. The source 24b, drain 25, channel forming region 26b, and gate 27b construct an n-channel MOS transistor T2b of an enhancement type.

Since the transistors T2a and T2b are formed on the well 22 and substrate 21 through the insulating film 23, respectively, capacitors are formed on the portions, respectively. Consequently, the circuit formed by both the

transistors T1a and T1b is as shown in Fig. 2. Reference symbols Ca and Cb denote the above capacitors. The potential of the power voltage Vdd is applied to the channel forming region 26a through the capacitor Ca and the potential of the substrate voltage Vss is applied to the channel forming region 26b via the capacitor Cb.

The embodiment fairly differs from the conventional CMOS shown in Fig. 3 in that the enhancement type MOS transistor T1a is replaced with the accumulation type MOS transistor T2a.

As mentioned above, in the transistor T2a, the channel forming region 26a is set to a p-type and the p-channel is formed in the accumulation mode. When an input level is set to H, the transistor has to be turned off and, when the input level is set to L, it has to be turned on. Since the source 24a and the drain 25 are formed so as to have an n^+-type, the P-N junction of the channel forming region 26a and the drain 25 is performed in the forward direction. On the contrary, the P-N junction of the channel forming region 26a and the source 24a is performed in the reverse direction. Therefore, in the portion between the p-channel formed in the channel forming region 26a and the source 24a, it is desirable that the presence or absence of breakdown depends on the above turn-on or turn-off.

The presence or absence of the breakdown is

discriminated in accordance with the magnitude of a hole density of the p-channel portion. Owing to the operation of the gate 27a, the hole density when the input level is set to L is larger than that when it is set to H. Therefore, it is sufficient to set the hole density of the p-channel portion so that the difference between the hole densities corresponding to L and H of the input level corresponds to the discrimination of the presence or absence of the breakdown.

In the transistor T2a, as mentioned above, the hole density is set by setting a dose amount of B in the channel forming region 26a to be higher than that in the channel forming region 26b in the transistor T2b and by applying the potential of the power voltage Vdd through the capacitor Ca. The setting also makes the operation to prevent that when the input level is set to H, the channel in the inversion mode is formed in the channel forming region 26a to turn on the transistor T2a.

Consequently, the CMOS according to the embodiment operates as shown in Table 2 and forms an inverter of a low electric power consumption in a manner similar to the conventional CMOS shown in Fig. 3.

Table 2 Operation of Embodiment

Input	State of T2a	State of T2b	Output
H	OFF	ON	L
L	ON	OFF	H

Since all of the sources 24a and 24b and the drain 25 are set to an n^+-type, the gates 27a and 27b, sources 24a and 24b, and drain 25 can be formed in a lump, respectively. Consequently, the manufacture is simplified as compared with the conventional CMOS and the N-P-N-P junction which causes latch-up is not also formed (in the N-P-N-P-N junction constructed by the source 24a, channel forming region 26a, drain 25, channel forming region 26b, and source 24b, since the drain 25 is set to an n^+-type, there is no problem).

From the above-mentioned explanation, the followings can be seen. That is:

(1) Since the capacitor Cb is accidentally formed because the embodiment shows the SOI structure, it is possible to provide no capacitor from the viewpoint of function.

(2) The well 22 and the capacitor Ca are provided toward the setting of the above-mentioned hole density in the channel forming region 26a. For the setting, the potential to be applied to the well 22 can be made

different from the power voltage Vdd. When the setting can be realized by adjusting the dose amount of B, the well 22 and the capacitor Ca are not needed. In this case, the manufacture is further simplified.

(3) Since the well 22 is one electrode of the capacitor Ca, it can be replaced with the other conductive electrode which is isolated from the substrate 21.

(4) The conductivity types of all of the semiconductor regions such as source, drain, channel forming region, and the like can be also opposite to those of the embodiment. In this case, the polarities of the power voltage Vdd and the substrate voltage Vss are set to the opposite polarities.

[Effects of the Invention]

As mentioned above, according to the construction of the invention, in the complementary MOS integrated circuit, the channel forming regions of the two transistors constructing the complementary type can be set to the same conductivity type, so that there is such an effect that the manufacture can be simplified and no generation of latch-up can be realized.

4. Brief Description of the Drawings

Fig. 1 is a schematic sectional side elevation view

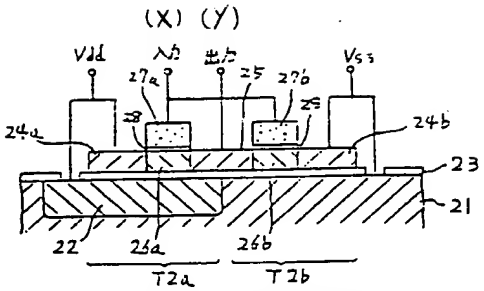
of an embodiment of the invention;

Fig. 2 is its circuit diagram;

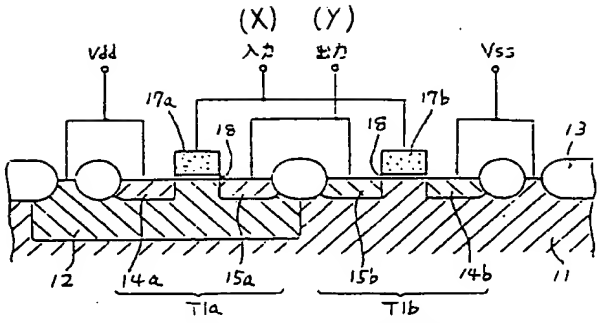
Fig. 3 is a schematic sectional side elevation view of an example of a conventional CMOS; and

Fig. 4 is its circuit diagram.

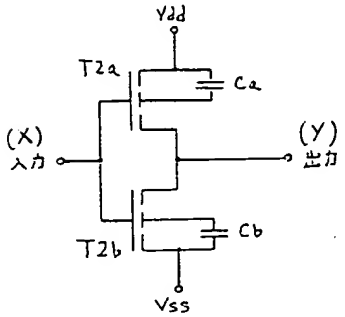
In the diagram, reference numerals 11 and 21 denote substrates; 12 and 22 wells; 13 a field insulating film; 23 an insulating film; 14a, 14b, 24a, and 24b sources; 15a, 15b, and 25 drains; 26a and 26b channel forming regions; 17a, 17b, 27a, and 27b gates; 18 and 28 gate insulating films; T1a an enhancement type p-channel MOS transistor; T2a an accumulation type p-channel MOS transistor; T1b and T2b enhancement type n-channel MOS transistors; Ca and Cb capacitors; Vdd a power voltage; and Vss a substrate voltage.



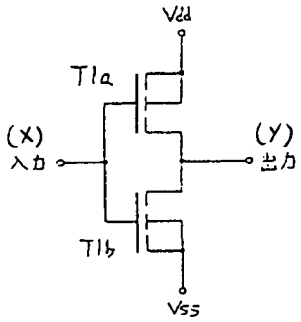
本発明実施例の模式断面図
第1図



従来のCMOS例の模式断面図
第3図



実施例の回路図
第2図



第3図例の回路図
第4図

[Fig. 1]

Schematic sectional side elevation view of embodiment of the invention

(x)… Input

(y)… Output

[Fig. 2]

Circuit diagram of embodiment

(x)… Input

(y)… Output

[Fig. 3]

Schematic sectional side elevation view of example of conventional CMOS

(x)… Input

(y)… Output

[Fig. 4]

Circuit diagram of example of Fig. 3

(x)… Input

(y)… Output